OPEN ACCESS

Spring International Engineering Research Journal: ISSN: 2384-5058

Volume-12 | Issue-12| Dec., Pp 38-,49, 2024 |

Research Papers

Prediction and Optimization of Material Chip size required to enhance the Tool Life of some selected Materials

[1]Eyituoyo Amorighoye Lucky, [1]Achebo Joseph, [2]Obahiagbon Kessington, *[1]Uwoghiren Frank Omos

[1]Department of Production Engineering, University of Benin, Benin City, Nigeria
[2]Department of Chemical Engineering, University of Benin, Benin City, Nigeria

Emails:genelee911@gmail.com,joseph.achebo@uniben.edu,kess.obahiagbon@uniben.edu,frank.uwoghiren@uniben.edu.
Corresponding author email: *frank.uwoghiren@uniben.edu.

Accepted: 23/8/2024

Abstract: Because of its exceptional mechanical qualities, pitting resistance, stress-corrosion cracking, production features, and uses in oil and gas, nuclear power, thermal power generation, chemical processing, saltwater treatment, and pipeline infrastructure, duplex stainless steel has emerged as one of the stainless steel family's fastest-growing materials. However, because of its great toughness, poor heat conductivity, and ductility, it is more challenging to process. In order to answer and meet the industrial need, the experiment was carried out utilizing 2205 Duplex Stainless Steel bars taking into account carbide cutting tools, estimating machining time employing a CNC lathe. The Central Composite Design was the experimental design adopted, that was produced using the design 7.1 software and the Response Surface Methodology achieved a desirability value of 0.973, indicating optimal machining conditions. These conditions included a depth of cut of 0.4, a cutting velocity of 250, and a feed rate of 0.5, yielded a machined component with a material chip size of 0.141. The ANN model was used in conjunction with the RSM model to forecast the output parameters. Due to its greater coefficient of determination, the Response Surface Methodology is chosen to be the superior predictive model over the Artificial Neural Network based on the data obtained.

Keywords:: *Chip size, Machining, Response surface methodology, Artificial neural network*

Published: x/8/2024 2024.

1. INTRODUCTION

In machining operations, the size and morphology of chips produced during the cutting process have a significant impact on tool life, machining efficiency, and surface finish (Das et al., 2022). Optimizing chip size is crucial in machining operations as it affects several aspects of the process. Smaller, well-controlled chips can result in lesser tool wear, lower cutting forces, increased surface quality, and increased overall machining efficiency. On the other hand, improper chip formation can cause tool damage, poor surface finish, and increased energy consumption (Tlhabadira et al., 2019). Different materials exhibit varying chip formation characteristics during machining. Altering cutting velocity, feed advancement, and cutting depth which are critical machining variables which affect chip size (Ghoreishi et al., 2018). Optimization approaches aim to get the ideal mixture of these parameters to achieve the desired response prediction as shown in Oyejide et al., 2024 where decision support expert techniques for Improved gasoline yield. Tool geometry, including rake angle and tool nose radius, can impact chip formation (Chaudhari and Wang, 2019). Optimization involves designing tool geometries that promote the formation of controlled and manageable chips. Proper coolant and lubrication systems can assist in chip control (Darshan et al., 2019). The optimization of temperature control and lubrication techniques contributes to reducing chip size and improving tool life. High-speed machining, trochoidal milling, and other advanced machining techniques are explored for their potential to influence chip size and enhance tool life. Gupta et al. (2019) found that the duration of interface between the device and the chip decreased as the speed of cut increased while Khawarizmi et al. (2022) estimated the thermal and strain characteristics within the chip by using finite element analysis to find the Johnson-Cook material model factors

that best reproduced the experimentally observed adiabatically sheared segmented chip morphology and intermittent cutting force fluctuations. Surface quality and tool life are decreased as a result of the continual chip issue brought on by varying rake angles and feed rates (Zamri & Yusoff, 2022). When turning ductile steels and super alloys, chip control challenges are frequently encountered during machining with varied depths of cut for finishing, semi-finishing, and roughing. To manage chips during the turning process, the majority of inserts use chip breaker geometry. Nevertheless, in the processing of deformable metals, intact chips continue to provide challenges for automation and production management (Yılmaz et al., 2018). Modelling output machining performances, fundamental factors (such as forces, temperatures, stresses, etc.) and machine industry-relevant output performances (such as tool life, surface quality, and chip formation, etc.) are crucial because traditional machining techniques continue to account for the majority of manufacture processes (Sekulic et al., 2018). Abhang et al. (2021) found that the primary determinant of chip thickness is feed rate, which is succeeded by cut depth and nose radius. Several experiments were carried out by Aamir et al. (2020) that were depending on the thrust force measurement, the post-drilling tool settings, chip development, and the hole quality as measured by surface roughness and burrs. According to the findings, small-diameter carbide drills with increased tip angles, yielded better-quality holes, minimized edge wear from shorter chip breaking, and less thrust force. In order to maintain operator safety and productivity, continual chip control in machining operations is a critical concern. Additionally, a CNC machine or automated production system requires effective chip control in particular because any chip control failure might result in a decrease in productivity (Yilmaz and Kiyak, 2020). Drilling uses a revolving cutter known as a drill to produce round holes in a workpiece. Chips vary in size and shape due to differences in drill design characteristics, machining settings, and material pairings between the tool and workpiece. Aamir et al. (2020) found that smaller, well-broken chips resulted in smoother drilling. They concluded that chip size, particularly length and thickness, significantly impacted the formation of high-quality holes and less tool wear. Continuous chips of excessive length tend to wrap around the drill, necessitating manual intervention and negatively impacting surface roughness (Ra). Furthermore, it was mentioned that the chips may also obstruct the drill grooves, breaking the tools and lengthening the machining time. Chip breakage is challenging when machining ductile steel and superalloys, and long chips are the primary issue with continuous turning operations. Chip formation during machining reduces operating efficiency and has a negative impact on workpiece quality, tool life, worker and tool safety, and energy usage. Chip breaking must be used to manage the ongoing chip generation during machining in order to mitigate such issues (Yılmaz et al., 2020). Optimizing material chip size is a critical aspect of machining operations with significant implications for tool life, efficiency, and product quality. It is a multidisciplinary field that involves considerations of cutting parameters, tool design, coolant/lubrication strategies, and material properties (Du et al., 2023). Advancements in chip size optimization benefit industries ranging from automotive manufacturing to aerospace and beyond.

2. METHODOLOGY

2.1 Experimental Approach

In this study, based on the number of model inputs, an empirical approach was adopted. The matrix was created utilizing software designed by a design expert. It made use of the CCD and the 2^k factorial design. The CCD accommodates 3-5 levels for input parameters, whereas the 2^k factorial design limits input parameters to two levels.

2.2 Method of Data Collection

In this study 20 runs of the experiment were produced by the central composite design, utilizing Design Expert 7.1, a layout was generated. This encompassed variables and responses; these experimental trials contained the outcomes of the chosen substance. Techniques from RSM and ANN were subsequently employed to analyze this matrix.

2.3 Response Surface Methodology (RSM)

RSM is extensively utilized in scenarios involving multiple input variables impacting one or multiple outcome variables. It integrates mathematical and statistical models to investigate systems where the objective is to improve a target response influenced by several variables. RSM assumes a crucial role in the creating, developing, and formulating new offerings, in addition to perfecting current ones. Its core elements comprise trial planning, statistical modeling, and enhancement methodologies, which collectively explore and establish the empirical relationships among factors.

2.4 Artificial Neural Network

A neural network is a distributed, massively parallel computing system that can store empirical data for a

variety of uses. It is an effective data mining technology that is mostly used to uncover hidden patterns in datasets. It's worth mentioning that neural networks and the human brain have two key parallels. First, synaptic weights—a measure of the intensity of neural connections —are used to store knowledge during the learning process. Second, a transfer function (f) computes the cumulative weighted input plus an offset value. Each fundamental neuron receiving R inputs allocates suitable weights (w). The transfer function (*f*) can be any differentiable function used to determine neuron outputs. In multilayer networks, the log-sigmoid transfer function, also referred to as logsig, is a commonly employed choice. The sigmoid transfer function, specifically the log-sigmoid, generates output values that range from 0 to 1 when the net input of the neuron shifts from a negative value to a positive infinity. Multilayer networks demonstrate the flexibility in selecting transfer functions, with some opting for the transfer function of tan-sigmoid. In many cases, sigmoid output neurons are preferred for tasks involving pattern recognition, while linear output neurons prove valuable when tackling function-fitting challenges.

3. FINDINGS AND ANALYSIS

3.1 Modelling and Optimization using RSM

Twenty experimental runs were conducted in this investigation, with each run determining the cut depth, spindle speed and feed rate. For each experiment the responses were measured.

Table 1 presents the cumulative sum of squares for the chip size response to verify model applicability.

Table 1: Cumulative Model Sum of Squares **chip size**

Origin	Squares Sum	df	Average Square	F-value	p-value	
Average vs Aggregate	1.30	1	1.30			
Linear vs Average	0.0138	3	0.0046	0.6055	0.6210	
2FI vs Linear	0.0669	3	0.0223	5.30	0.0132	
Quadratic vs 2FI	**0.0524**	**3**	**0.0175**	**75.93**	**< 0.0001**	**Recommended**
Cubic vs Quadratic	0.0009	4	0.0002	1.03	0.4637	Aliased
Residual	0.0014	6	0.0002			
Aggregate	1.43	20	0.0715			

Choose the highest-order polynomial where the model remains unbiased and the extra terms are statistically significant.

A test for lack of fit showed performed to determine which model was best suited for Chip Size, and the model with the least amount of lack of fit was selected. Table 2 displays the lack of fit results for Chip Size.

Table 2: Lack of Fit Tests for chip size

Origin	Squares Sum	df	Average Square	F-value	p-value	
Linear	0.1203	12	0.0109	41.03	0.0004	
2FI	0.0534	9	0.0067	25.04	0.0013	
Quadratic	**0.0010**	**5**	**0.0002**	**0.7266**	**0.6327**	**Recommended**
Cubic	0.0000	1	0.0000	0.1221	0.7410	Aliased
Residual Error	0.0013	6	0.0003			

A negligible lack-of-fit should be present in the chosen model.

The model summary statistics for Chip Size were assessed in order to further verify the model's applicability; the model with the largest R-squared value is the one that is preferred. Summary statistics for the model of the chip size is as shown in table 3

Table 3: Summary statistics for chip size

Origin	Std. Dev.	R^2	Adjusted R^2	Predicted R^2	PRESS	
Linear	0.0872	0.1020	-0.0664	-0.6282	0.2206	
2FI	0.0649	0.5960	0.4095	0.2000	0.1084	
Quadratic	**0.0152**	**0.9830**	**0.9677**	**0.9279**	**0.0098**	**Recommended**
Cubic	0.0151	0.9899	0.9681	0.9329	0.0091	Aliased

Examine the model that maximizes both the **Predicted R^2** and the **Adjusted R^2**.

The model's ANOVA was calculated to further check for the significance in the quadratic framework, the analysis of variance (ANOVA) was conducted for Chip Size. This is displayed in Table 4.

Table 4: Quadratic Model ANOVA for **chip size**

Origin	Squares Sum	Df	Average Square	F-value	p-value	
Model	0.1332	9	0.0148	64.29	< 0.0001	Important
A-depth of cut	0.0044	1	0.0044	19.02	0.0014	
B-cutting speed	0.0000	1	0.0000	0.1777	0.6823	
C-feed rate	0.0094	1	0.0094	40.81	< 0.0001	
AB	0.0003	1	0.0003	1.36	0.2710	
AC	0.0666	1	0.0666	289.35	< 0.0001	
BC	0.0000	1	0.0000	0.0543	0.8204	
A^2	0.0129	1	0.0129	56.22	< 0.0001	
B^2	0.0200	1	0.0200	86.66	< 0.0001	
C^2	0.0163	1	0.0163	70.98	< 0.0001	
Residual	0.0023	11	0.0002			
Lack of Fit	0.0010	6	0.0002	0.7266	0.6327	not important
Residual Error	0.0013	6	0.0003			
Cor Aggregate	0.1355	18				

The Model F-value of 64.29 reveals the framework's strong statistical importance, with merely a 0.01% probability that it may be attributed to random noise. P-values less than 0.0500 signify important framework terms, and here, factors A, C, AC, A^2, B^2, and C^2 are important. In contrast, P-values surpassing 0.1000 suggest that the corresponding framework terms are not important. If the framework contains numerous non-significant terms (apart from those needed to maintain hierarchy), simplifying the framework may improve its accuracy.

The Lack of Fit F-value of 0.73 indicates that the Lack of Fit is statistically insignificant relative to residual error, with a 63.27% probability of a result of this kind arising from noise. This outcome is favorable, as it implies the model accurately represents the data.

To evaluate the robustness and reliability of the developed model, a goodness-of-fit statistical test is performed for chip size as shown in Table 5.

Table 5: Statistical Measures of Fit for Chip Size

Std. Dev.	0.0152	**R^2**	0.9830
Average	0.2545	**Adjusted R^2**	0.9677
C.V. %	5.96	**Predicted R^2**	0.9279
		Adeq Precision	24.4287

There is good agreement between the Predicted R^2 value (0.9279) and the Adjusted R^2 value (0.9677), since the difference is minimal (less than 0.2). This consistency indicates a reliable model.

Adequate Precision, quantifying the signal-to-noise ratio indicates a favorable outcome when it exceeds 4. The obtained ratio of 24.429 confirms a robust signal, confirming the model's reliability for exploring the design space.

To optimize the chip size, the coefficient estimates are determined, and the statistical details of these estimates are summarized in Table 6.

Table 6: Coefficient Estimate Statistics for the Chip Size

Factor	Coefficient Estimate	df	Standard Error	95% CI Low	95% CI High	VIF
Intercept	0.2266	1	0.0062	0.2128	0.2404	
A-depth of cut	0.0179	1	0.0041	0.0088	0.0271	1.001
B-cutting speed	0.0017	1	0.0041	-0.0074	0.0109	1.001
C-feed rate	0.0262	1	0.0041	0.0171	0.0354	1.001
AB	-0.0063	1	0.0054	-0.0182	0.0057	1.001
AC	-0.0912	1	0.0054	-0.1032	-0.0793	1.001
BC	-0.0013	1	0.0054	-0.0132	0.0107	1.001
A^2	-0.0300	1	0.0040	-0.0389	-0.0211	1.02
B^2	0.0372	1	0.0040	0.0283	0.0461	1.02
C^2	0.0337	1	0.0040	0.0248	0.0426	1.02

In an orthogonal design, the intercept signifies the overall mean response. Coefficient estimates subsequently reveal the anticipated alteration in reaction to a single-unit shift in a factor, while maintaining all else being equal. Essentially, these coefficients represent refinements to the mean response based on specific factor configurations. VIFs are one when the factors are independent; multicollinearity is suggested by Variance Inflation Factors (VIFs) exceeding 1; the more severe the correlation between the factors, the higher the VIF. Generally speaking, VIFs under 10 are acceptable.

A normal plot of residuals is demonstrated that the model is appropriate for the data on Chip Size as shown in Figure 1

.

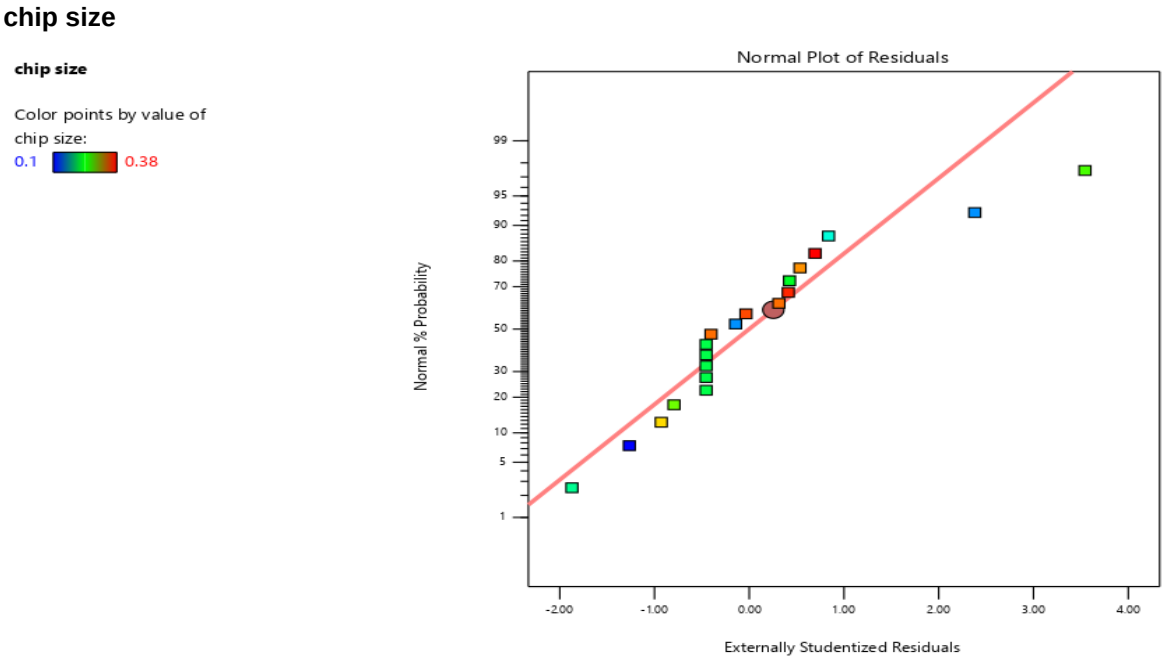

Figure 1: Residual Normality Plot for Chip Size

If residuals are normally distributed, the points will lie along a straight line, as shown by the normal probability plot. Even a regular set of data can have a modest scatter. The typical residual plot A moderate scatter was found by Chip Size, suggesting that the data is normal.

A plot of residuals and the projected value for Chip Size was created in order to look for big patterns or expanding variance, as seen in Figure 2.

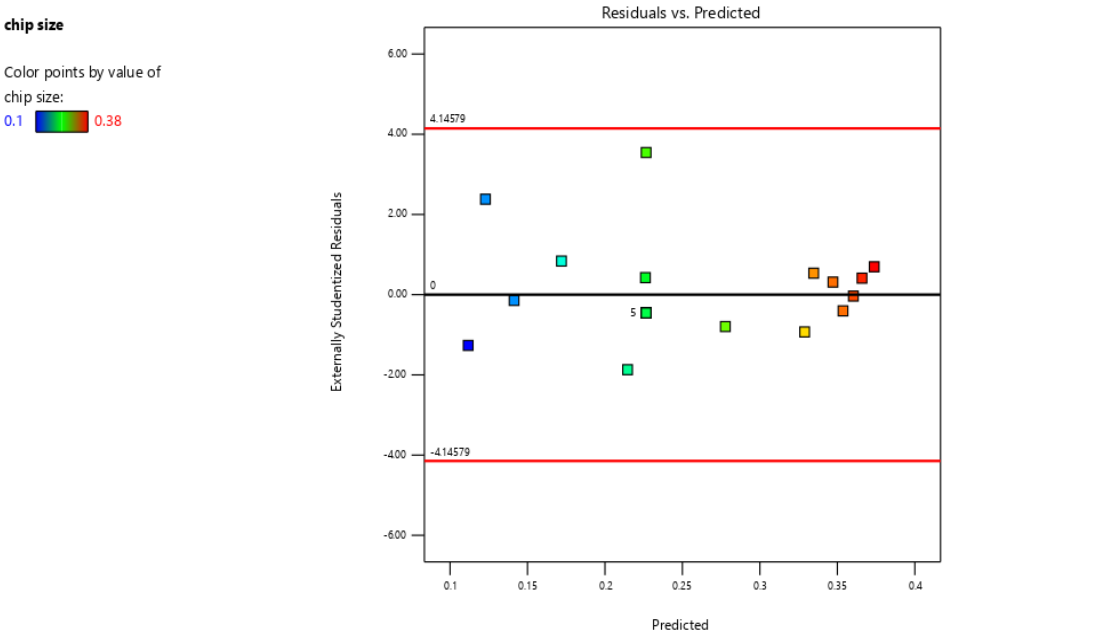

Figure 2: Residuals vs. Predicted plot for Chip Size

Plot of cook's distance for Chip Size was constructed to identify any potential any unusual patterns in the data. The change in the regression equation if the outlier were deleted from the analysis is known as the cook's distance. An outlier should be looked into if a point has a significantly large distance from the other data points. Figure 3 displays the calculated Cook's distance for Chip Size.

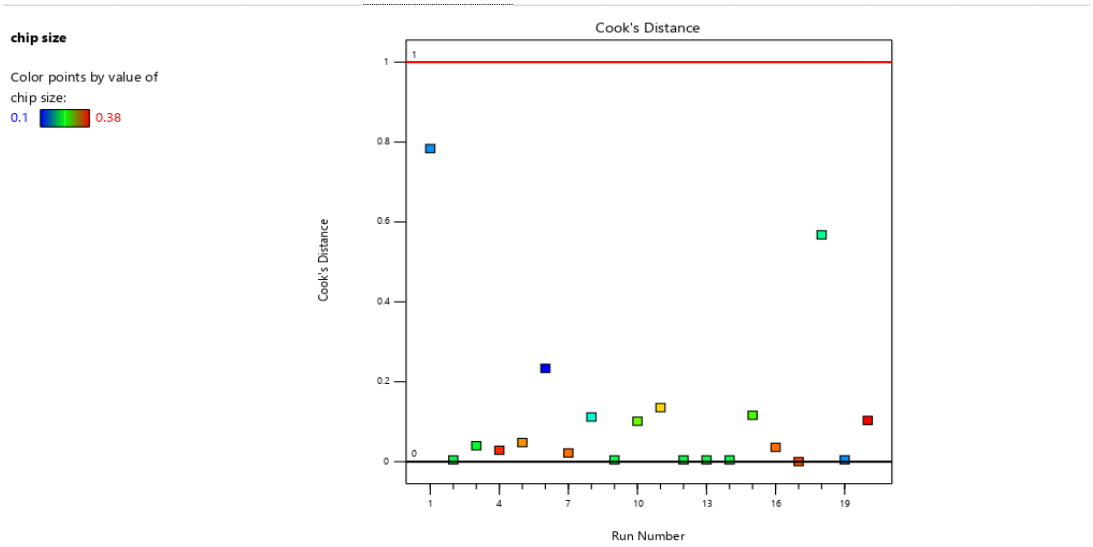

Figure 3: Cook Distance for Chip Size

Box-Cox plot of Power Transforms is used to reduce anomalies such as non-additivity, non-normality and heteroscedasticity. It modifies a set of data's distributional form to be more regularly distributed in order to apply tests and confidence limits that depend on normality.

For Chip Size, as illustrated in Figure 4, the fitted values are displayed against the observed values to detect any values that are difficult for the model to detect.

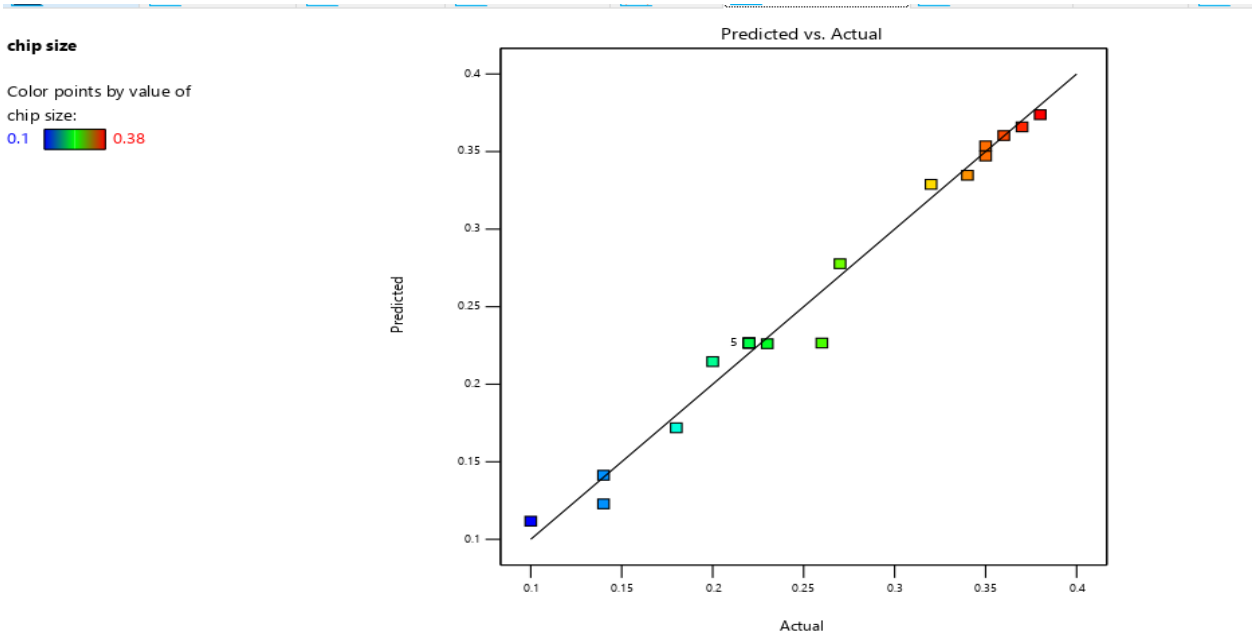

Figure 4: Plot of Predicted Versus Actual for Chip Size

The graph shows that the spots are near the line of fit. In essence, the model can forecast the majority of the data points.

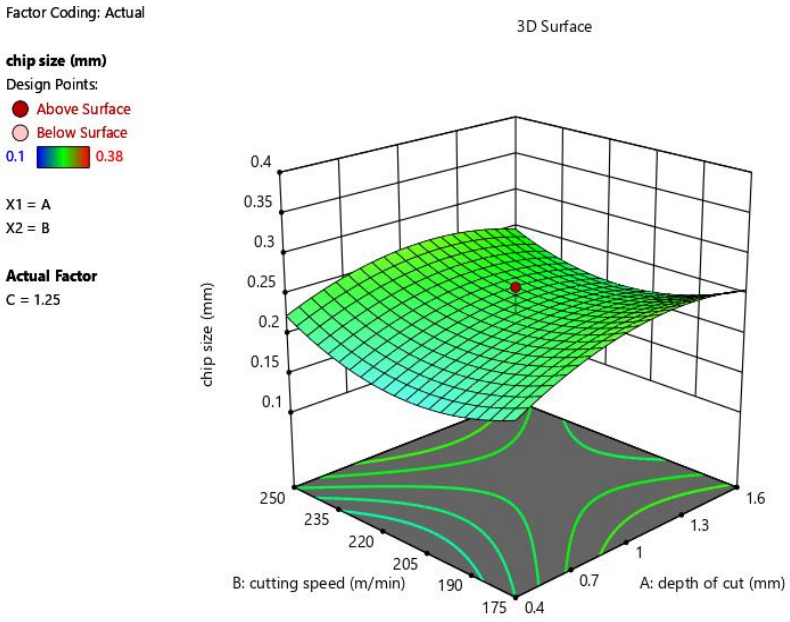

Figure 5: Cutting Speed and Cutting Depth Effect on Chip Size

The Surface Plot which shows the impact of Cutting Velocity and Cutting Depth on the Chip Size reveals that a rise in Cutting Velocity results in a moderate increase and decrease in the Chip Size while a rise in Cutting Depth results in a the direct increase of the Chip size.

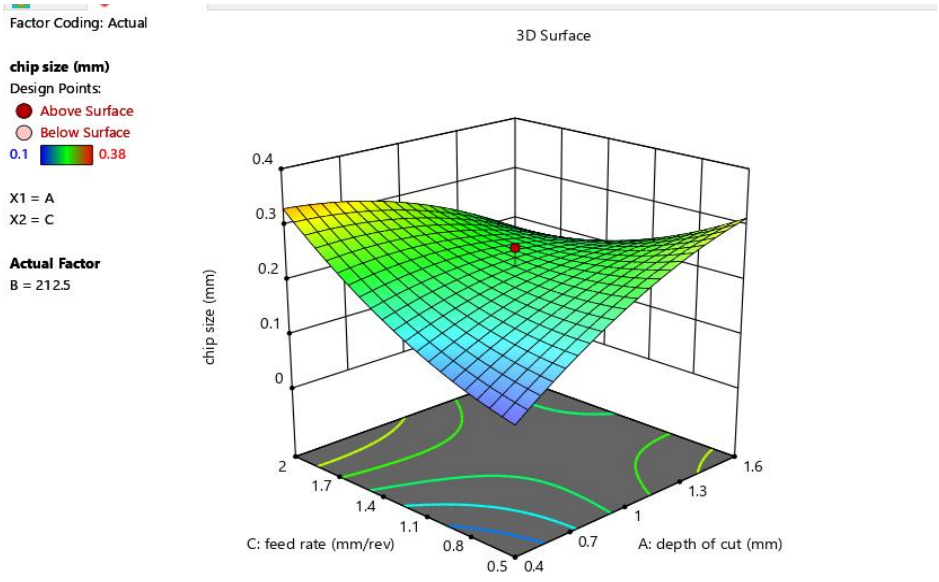

Figure 6: Machining Rate and Cutting Depth Effect on Chip Size

The Surface Plot which demonstrates how the depth of cut and feed rate affect the Chip Size reveals that rise in Machining Rate and Depth of Cut results in an rise in Chip Size. But the Feed Rate has a higher impact on the Chip Size.

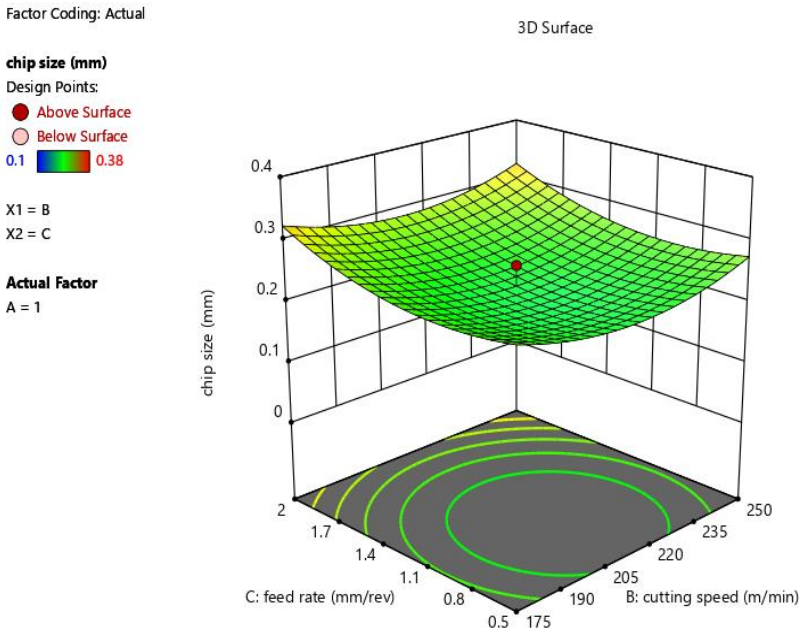

Figure 7: Effect of Machining Rate and Cutting Speed on Chip Size

The Surface Plot which shows the effect of Feed Rate and Cutting Speed on the Chip Size shows that a rise in Machining Rate leads to a higher Chip Size whereas a rise in Cutting Speed leads to slight reduction and increase of the Chip Size.

3.2 Modelling and forecasting employing ANN

The ANN study is conducted using Matlab R2022a. The Data is saved in the folder of the matlab, then normalized by converting to Numeric Matrix form. This will dynamically select the dataset's range, and Matlab will load the data using import selection. In Matlab, APPS is selected, then Neural Net Fitting to be begin the analysis process. The Levenberg-Marquardt Backpropagation algorithm technique, commonly referred to as an improved quadratic gradient optimization technique, was determined to be the superior learning algorithm and used in the network architecture design. Alternate numbers of hidden neurons were used in order to build a neural network optimized via the Levenberg- Marquardt Backpropagation algorithm to know the precise number of hidden neurons. The hidden layer consisted of 8 neurons, and the network outcome was tracked using coefficient of determination (r2) and MSE. In the network's input layer, the hyperbolic tangent (tan-sigmoid) function is applied to compute the layer's output based on the network's input, whereas the output layer employs a linear activation function (purelin). The network generation process divides the sample data for training data sets, verification and to test. For this study, 70% of the data was employed to perform the network training, 15% for verifying the network while the rest 15% was used to test the performance of the network at a maximum training cycle of 1000 epochs was used. Weight and bias values are optimized using the Trainlm function, which employs Levenberg-Marquardt algorithm. Despite using greater memory than other methods, Trainlm is one of the fastest backpropagation methods, making it a top recommended supervised learning algorithm.

The ANN architecture is 3-8-1, the network architecture produced by the back propagation neural network for material chip size prediction.

Figure 8 shows a performance metrics graph tracking the progress of training, verification, and testing.

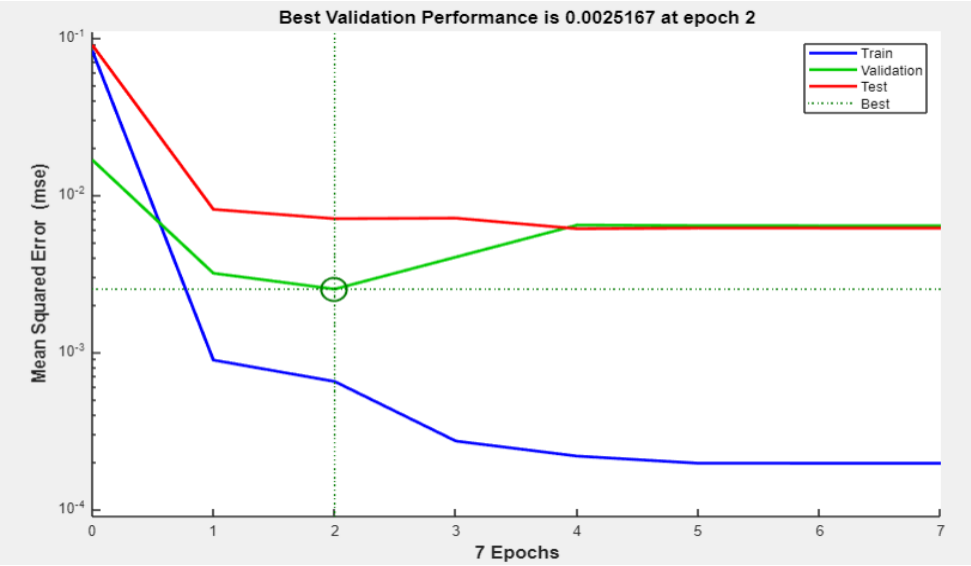

Figure 8: Model Performance Plot for Predicting Material Chip Size

The performance plot in Figure 8 exhibits no signs of overfitting. Furthermore, the training, validation, and testing curves exhibit a similar trend, which aligns with expectations as the raw data were normalized prior to being used. A lower mean square error (MSE) is a critical measure of the network's training accuracy. An error rate of 0.0025167 observed at epoch 2 demonstrates the network's strong predictive capability for material chip size.

The training status, which includes details of the gradient evaluation, update gain (Mu), and validation test, is illustrated in Figure 9, providing further insight into the model's training dynamics.

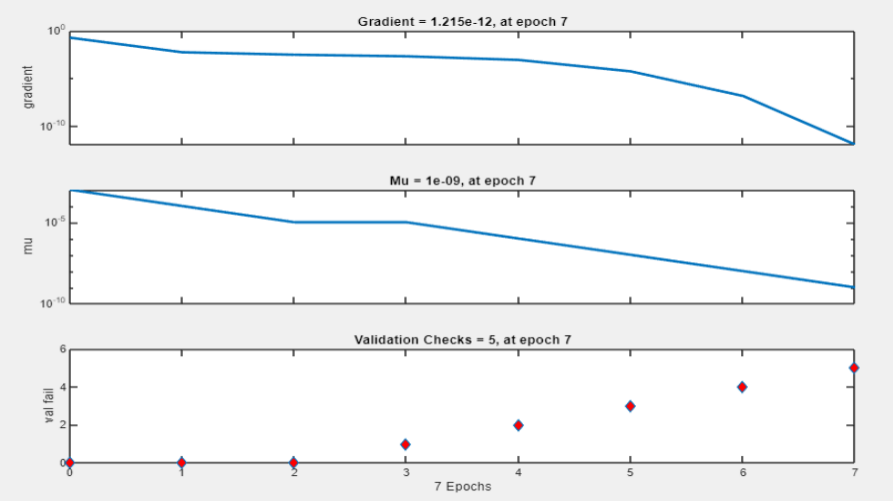

Figure 9: Training Status of Neural Network for Predicting Material Chip Size

Artificial neural networks use back propagation to determine each neuron's error contribution subsequent to executing a subset of learning data. The neural network determines the derivative of the loss function to quantify the proportion of error for each selected neuron. A smaller mistake is preferable. Figure 9's computed gradient value of 1.215e-12 shows that each chosen neuron's error contribution is extremely small. The neural network training algorithm's control parameter is called momentum gain (Mu). The value of the training gains must be smaller than unity. A network with a strong capacity to forecast the material chip size is demonstrated

by momentum gains of 1e-07. The regression chart that displays the relationship between the input variables (DOC, cutting speed and feed rate) and the target variable (material chip size) together with the training, verification, and testing processes, is shown in Figure 10.

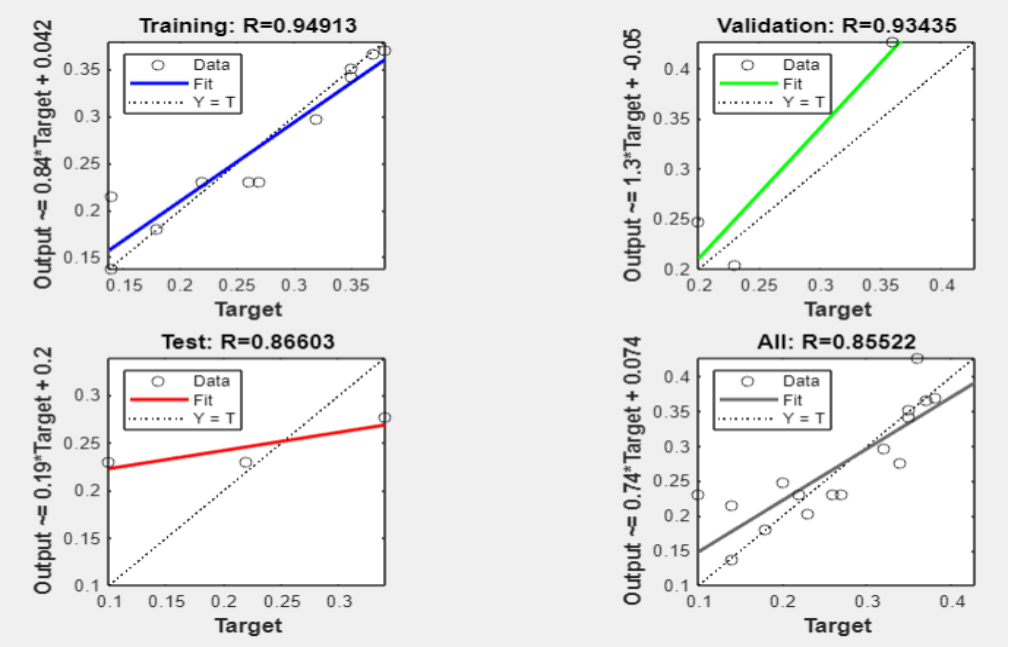

Figure 10: Training, Validation, and Testing Progress Regression Chart

4. CONCLUSION

The useful service life of a machined engineering structure is affected by its chip size. In this study, creation of numerical models utilizing response surface methodology and artificial neural network for optimizing and forecasting the chip size, taking into account the feed rate, cutting speed, and depth of cut as predictors. In order to create a machined structure with a material chip size of 0.141, the RSM analysis revealed optimal parameters: 0.400 depth of cut, 250.000 cutting speed, and 0.500 feed rate, with a desirability score of 0.973. The experimental design that was chosen was the central composite design, which was created using the design 7.1 software. The artificial neural network model was used in conjunction with the RSM methodology to forecast the output parameters. The response surface methodology was deemed the most effective prediction framework according to results over the Artificial Neural Network as a result of its greater coefficient of determination.

REFERENCES

Aamir, M., Tolouei-Rad, M., Giasin, K., & Vafadar, A. (2020). Feasibility of tool configuration and the effect of tool material, and tool geometry in multi-hole simultaneous drilling of Al2024. *The International Journal of Advanced Manufacturing Technology*, *111*, 861-879.

Aamir, M., Tu, S., Giasin, K., & Tolouei-Rad, M. (2020). Multi-hole simultaneous drilling of aluminium alloy: A preliminary study and evaluation against one-shot drilling process. *Journal of Materials Research and Technology*, *9*(3), 3994-4006.

Abhang, L. B., Iqbal, M., & Hameedullah, M. (2021). An Experimental Model for the Prediction of Chip Thickness in Steel Turning. In *Proceedings of the 2nd International Conference on Experimental and Computational Mechanics in Engineering: ICECME 2020, Banda Aceh, October 13–14* (pp. 137-149). Springer Singapore.

Chaudhari, A., & Wang, H. (2019). Effect of surface-active media on chip formation in micromachining. *Journal of Materials Processing Technology*, *271*, 325-335.

Darshan, C., Jain, S., Dogra, M., Gupta, M. K., Mia, M., & Haque, R. (2019). Influence of dry and solid lubricant-assisted MQL cooling conditions on the machinability of

Inconel 718 alloy with textured tool. *The International Journal of Advanced Manufacturing Technology*, *105*, 1835-1849.

Das, A., Kamal, M., Das, S. R., Patel, S. K., Panda, A., Rafighi, M., & Biswal, B. B. (2022). Comparative assessment between AlTiN and AlTiSiN coated carbide tools towards machinability improvement of AISI D6 steel in dry hard turning. *Proceedings of the Institution of Mechanical Engineers, Part C: Journal of Mechanical Engineering Science*, *236*(6), 3174-3197.

Du, Y., Lu, M., Lin, J., & Yang, Y. (2023). Experimental and simulation study of ultrasonic elliptical vibration cutting SiCp/Al composites: chip formation and surface integrity study. *Journal of Materials Research and Technology*, *22*, 1595-1609.

Ghoreishi, R., Roohi, A. H., & Ghadikolaei, A. D. (2018). Analysis of the influence of cutting parameters on surface roughness and cutting forces in high speed face milling of Al/SiC MMC. *Materials Research Express*, *5*(8), 086521.

Gupta, M.K., Mia, M., Pruncu, C.I., Kapłonek, W., Nadolny, K., Patra, K., Mikolajczyk, T., Pimenov, D.Y., Sarikaya, M. and Sharma, V.S., 2019. Parametric optimization and process capability analysis for machining of nickel-based superalloy. *The International Journal of Advanced Manufacturing Technology*, *102*, pp.3995-4009.

Khawarizmi, R. M., Lu, J., Nguyen, D. S., Bieler, T. R., & Kwon, P. (2022). The Effect of Ti-6Al-4V Microstructure, Cutting Speed, and Adiabatic Heating on Segmented Chip Formation and Tool Life. *Jom*, *74*(2), 526-534.

Kumar, B. S., Baskar, N., & Rajaguru, K. (2020). Drilling operation: A review. *Materials Today: Proceedings*, *21*, 926-933.

Oyejide O J, Faiz A, Muhammad A and Okwu M O 2024 Application of Decision Support Expert Systems for Improved gasoline yield in Refinery Catalytic Cracking *Procedia Comput Sci* **232** 3044–53

Sekulic, M., Pejic, V., Brezocnik, M., Gostimirović, M., & Hadzistevic, M. (2018). Prediction of surface roughness in the ball-end milling process using response surface methodology, genetic algorithms, and grey wolf optimizer algorithm. *Advances in Production Engineering & Management*, *13*(1), 18-30.

Tlhabadira, I., Daniyan, I. A., Machaka, R., Machio, C., Masu, L., & VanStaden, L. R. (2019). Modelling and optimization of surface roughness during AISI P20 milling process using Taguchi method. *The International Journal of Advanced Manufacturing Technology*, *102*, 3707-3718.

Yılmaz, B., Karabulut, Ş., & Güllü, A. (2018). Performance analysis of new external chip breaker for efficient machining of Inconel 718 and optimization of the cutting parameters. *Journal of Manufacturing Processes*, *32*, 553-563.

Yılmaz, B., Karabulut, Ş., & Güllü, A. (2020). A review of the chip breaking methods for continuous chips in turning. *Journal of Manufacturing Processes*, *49*, 50-69.

Yilmaz, Y., & Kiyak, M. (2020). Investigation of chip breaker and its effect in turning operations. *Journal of Advances in Manufacturing Engineering*, *1*(1), 29-37.

Zamri, M. F., & Yusoff, A. R. (2022). Effect of rake angle and feed rate on tool wear and surface topography for different chip size in machining carbon steels. *Jurnal Tribologi*, *34*, 1-11.